is formed over the plurality of drain electrodes, the plurality of source electrodes and the gate insulating layer; and

etching at least one of the passivation layer and the gate insulating layer to form [the plurality of] at least one second via hole[s], the first and second via holes exposing at least one of a portion of the plurality of drain electrodes, a portion of the plurality of source electrodes and a portion of the plurality of gate lines.

Claim 9, line 17, delete "etched".

REMARKS

Claims 1-13 are pending in this application. By this Amendment, claims 1, 2 and 9 are amended. Favorable reconsideration in view of the foregoing amendments and following remarks is respectfully requested.

Applicants appreciate an indication of allowable subject matter in claims 5 and 10-11, if rewritten in independent form to include all of the features of the base claims and any intervening claims. At this time, Applicants do not feel it is necessary to rewrite claims 5 and 10-11 in independent form given the following remarks.

The drawings are objected to under 37 C.F.R. §1.84(f) because they do not include certain reference signs mentioned in the description. By this Amendment, Applicants have amended the specification to clarify the location of element "172" in Fig. 5. Also, Applicants file herewith a Request for Approval of Drawing Corrections to correct Figs. 3B and 3C. Upon receipt of a formal Notice of Allowance, Applicants will submit formal drawings. Withdrawal of the objection is respectfully requested.

Claims 1-4, 6-7, 9 and 12 are rejected under 35 U.S.C. §103 as being unpatentable over Naito (U.S. Patent No. 5,334,860) in view of Hayashi et al. (U.S. Patent No. 5,208,690). This rejection is respectfully traversed.

Applicants' claimed invention is drawn to a method for manufacturing an active matrix liquid crystal device using five masks and an active matrix liquid crystal device produced therefrom. Applicants' claimed method comprises the following claim features: forming a plurality of gate electrodes over a substrate using a first mask; forming a plurality of etch stoppers over the plurality of gate electrodes using a second mask, each etch stopper being formed over one gate electrode; forming a plurality of drain electrodes and a plurality of source electrodes using a third mask, portions of each drain electrode and each source electrode being formed over a corresponding one of the etch stoppers, wherein the source and the drain electrode are separated over the corresponding one of the etch stoppers; forming over the substrate a passivation layer having at least one first via hole using a fourth mask; and forming a pixel electrode over the passivation layer using a fifth mask.

Applicants' claimed active matrix liquid crystal device comprises the following claimed features: a plurality of gate electrodes formed over a substrate and a plurality of gate lines formed over the substrate using a first mask; a plurality of etch stoppers formed over the plurality of gate electrodes using a second mask, each etch stopper formed over one gate electrode; a gate insulation layer formed over the substrate and the plurality of gate lines; a plurality of drain electrodes and a

plurality of source electrodes formed using a third mask, portions of each of the drain electrodes and the source electrodes being formed over a corresponding one of the etch stoppers, wherein the source and the drain electrodes are separated over the corresponding one of the etch stoppers; a passivation layer formed over the substrate, wherein the passivation layer is formed over the plurality of drain electrodes, the plurality of source electrodes and the gate insulation layer; and a plurality of via holes through at least one of the passivation layer and the gate insulation layer exposing at least one of a portion of the plurality of drain electrodes, a portion of the plurality of source electrodes, and a portion of the plurality of gate lines.

Naito teaches a method for making a panel used for forming an active matrix liquid crystal display device and the panel made therefrom. As depicted in Fig. 6, the panel of Naito is formed by a method comprising a minimum of eight masks. A four mask process is necessary to form the gate electrode, G_1, on substrate 11. A fifth mask is necessary for forming layer 16, an I-type semiconductor layer made of amorphous silicon. Moreover, a three mask process is necessary to form the drain electrode, D_1, on a gate insulating layer, 15, and semiconductor layer 16.

Naito fails to teach or suggest at least the following features of Applicants' claimed method: (1) a method for manufacturing an active matrix liquid crystal device using five masks; (2) forming a plurality of drain electrodes and a plurality of source electrodes using a third mask; (3) forming

over the substrate a passivation layer having at least one first via hole using a fourth mask; and (4) forming a pixel electrode over the passivation layer using a fifth mask.

Naito fails to teach or suggest at least the following features of Applicants' claimed active matrix liquid crystal device: (1) a passivation layer formed over the substrate wherein the passivation layer is formed over a plurality of drain electrodes, a plurality of source electrodes and a gate insulating layer; and (2) a plurality of via holes through at least one of the passivation layer and the gate insulating layer exposing at least one of a portion of the plurality of drain electrodes, a portion of the plurality of source electrodes and a portion of the plurality of gate lines.

The Examiner relies on the secondary teaching of Hayashi to cure the above-noted deficiencies of Naito. Hayashi teaches a liquid crystal display having a plurality of pixels with switching transistors. As depicted in Fig. 5, Hayashi teaches a method of forming a liquid crystal display using a minimum of five masks. A first mask forms a polycrystalline silicone layer 8. A second mask forms a gate insulating layer 9 and a gate electrode 5G. Third and fourth masks form insulating layers 10 and 11. A fifth mask forms pixel electrode 1.

Hayashi fails to teach or suggest at least the following features of Applicants' claimed method: (1) forming a plurality of gate electrodes using a first mask; (2) forming a plurality of etch stoppers over gate electrodes using a second mask; (3) forming a plurality of drain electrodes and a plurality

of source electrodes using a third mask; (4) forming a passivation layer having at least one first via hole therein using a fourth mask; and (5) forming a pixel electrode over the above mentioned passivation layer using a fifth mask.

Hayashi fails to teach or suggest at least the following features of Applicants' claimed active matrix liquid crystal device: (1) a plurality of etch stoppers over a plurality of gate electrodes; (2) a plurality of drain electrodes and a plurality of source electrodes, portions of each being separately disposed over an etch stopper; and (3) a passivation layer formed over the drain electrodes, source electrodes and a gate insulation layer.

The teaching of Hayashi is relied upon by the Examiner to show the incorporation of via holes in a liquid crystal display whereby pixel electrodes are connected to a switching transistor. The Examiner alleges that one of ordinary skill in the art, given the teaching of Hayashi, would have been motivated to first, form a passivation layer having via holes therein on the panel of Naito using a fourth mask, second, form at least one via hole through a passivation layer in order to form contact between a pixel electrode and at least one of a portion of the plurality of drain electrodes, a portion of the plurality of source electrodes, and a portion of the plurality of gate lines, and third, vary etching rates when forming via holes through passivation and gate insulation layers. Applicants disagree.

The teachings of Naito and Hayashi, taken alone or in combination, fail to teach or suggest Applicants' claimed invention. The combined teachings of Naito and Hayashi fail to

teach a method of making an active matrix liquid crystal device using five masks wherein each mask forms a particular claimed feature of Applicants' claimed invention. The combined teachings would result in a method comprising at least nine masking steps (eight from Naito and one from Hayashi), wherein the nine masking steps produced a product which lacks specifically located components such as drain electrodes, source electrodes and etch stoppers.

Moreover, the combined teachings of Naito and Hayashi fail to teach or suggest a device comprising Applicants' claimed features. For example, Naito and Hayashi fail to teach a passivation layer. The Examiner alleges that Hayashi teaches a passivation layer and that such a layer would have been obvious to one of ordinary skill in the art on the panel of Naito. Applicants disagree. Even if Hayashi teaches or suggests a passivation layer, neither Naito or Hayashi suggest to one of ordinary skill in the art where such a passivation layer would be formed on the panel of Naito. Furthermore, the combined teachings of Naito and Hayashi fail to teach or suggest via holes within such a passivation layer, particularly, via holes through such a passivation layer in order to expose a portion of a drain electrode, source electrode or gate line.

The only motivation for forming contact holes in the crystal display of Hayashi is to provide a connection between a pixel electrode and a switching transistor. Such motivation would be useless in the teaching of Naito due to the absence of such a switching transistor, as taught by Hayashi. Such a via

hole in the teaching of Naito would result in a connection between pixel electrode 12 and substrate 11 (See Fig. 6).

For the reasons given above, Applicants' submit that independent claims 1 and 9 define patentable subject matter. Furthermore, because claims 2-4, 6-7 and 12 depend from independent claims 1 and 9 and recite additional features Applicants submit that these claims also define patentable subject matter. Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 8 and 13 are rejected under 35 U.S.C. §103 as being unpatentable over Naito in view of Hayashi, as applied to claims 1-4, 6-7, 9 and 12 above, and further in view of Kaganowicz et al. (U.S. Patent No. 4,717,631) and Iwasaki et al. (U.S. Patent No. 5,316,956). This rejection is respectfully traversed.

Claim 8, which depends from claim 1, and claim 13, which depends from claim 9, further recite, respectively, a method of making an active matrix liquid crystal device using five masks wherein the passivation layer comprises silicon oxynitride formed at a temperature of about 200°C and a device produced thereby. Because claims 8 and 13 depend from claims 1 and 9, Applicants submit that claims 8 and 13 define patentable subject matter for at least the reasons given above in regard to claims 1 and 9.

In addition to the above-mentioned deficiencies, the combined teachings of Naito and Hayashi, fail to teach or suggest the additional feature recited in claims 8 and 13. Kaganowicz and Iwasaki fail to cure these deficiencies.

Kaganowicz and Iwasaki teach semiconductors comprising at least one silicon oxynitride passivation layer. Kaganowicz and Iwasaki do not teach or suggest the use of such a passivation layer in a method for manufacturing an active matrix liquid crystal device using up to five masks or in an active matrix liquid crystal device comprising Applicants' claimed features.

The Examiner alleges that because Kaganowicz and Iwasaki teach passivation layers as claimed by Applicants, it would have been obvious to one of ordinary skill in the art to substitute such a layer into the combined teachings of Naito and Hayashi. Applicants submit that there is no teaching or suggestion for such a combination, other than Applicants' disclosure. Moreover, even if the combination of references is proper, the combination fails to teach or suggest Applicants' claimed invention for the reasons given above.

Naito and Hayashi, taken alone or in combination, would not have suggested to one of ordinary skill in the art to seek the teaching of Kaganowicz or Iwasaki because Naito and Hayashi fail to teach or suggest passivation layers. The Examiner fails to point to any portion of the references that provides motivation to one of ordinary skill in the art to combine the references. The Examiner merely concludes that one of ordinary skill in the art would have been motivated to modify the panel formed by the combined teachings of Naito and Hayashi by substituting a passivation layer as taught by Kaganowicz or Iwasaki into the panel. Applicant submits that the Examiner has failed to provide a *prima facie* case of obviousness.

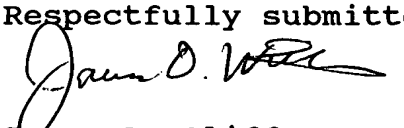
Accordingly, withdrawal of the rejection is respectfully solicited.

In view of the foregoing amendments and remarks, Applicants respectfully submit that all of claims 1-13 are in condition for allowance. Favorable reconsideration and prompt allowance of the claims are respectfully requested.

Applicants respectfully request Examiner Ton to return a fully initialled copy of the PTO-1449 filed August 28, 1995. (The PTO-1449 sent with the Office Action did not include the Examiner's initials).

Should the Examiner believe that anything further is necessary in order to place the application in condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,



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